Exploration of Pinned Photodiode Radiation Hardening Solutions Through TCAD Simulations

Olivier Marcelot Vincent Goiffon and Pierre Magnan

***Abstract*—The use of pinned photodiode (PPD) based CMOS image sensors in harsh radiation environment (such as space) is limited by their tolerance to ionizing radiation. Technology computer aided design (TCAD) simulations are performed to reproduce the radiation induced defect and therefore the dark current increase in pinned photodiode pixels up to 1 kGy (i.e. 100 krad) of total ionizing dose (TID). To do so, the TCAD models are calibrated with measurements performed on irradiated pixels. Then, the influence on the PPD radiation hardness of various manufacturing process and pixel design modifications is explored. This works shows that the proposed modification can improve the radiation hardness of pinned photodiode CMOS image sensors against ionizing.**

***Index Terms*—CMOS Image Sensors, CIS, Simulation, CMOS, pinned photodiode, PPD, Radiation effects, dark current, radiation hardening, Total Ionizing Dose, TID.**

I. Introduction

PINNED Photodiode (PPD) CMOS image sensors (CIS) are widely used in many products ranging from smartphones to scientific applications. Due to the continual technology improvement and to a better understanding of the device operation [1], [2], PPDs achieve now very high performances and overcome Charge Coupled Devices (CCD) in more and more challenging applications such as astronomy or earth observation. Compared to the simpler 3T pixels based on a conventional photodiode [3], PPD pixels include at least one more transistor which allows the charge transfer from a buried photodiode isolated from the surface oxide by the pinned P+ layer, to the floating node [4]. Then, a classical readout circuitry [5] transforms the potential drop of the floating node into a useful signal. The main advantages of this specific design are a very low dark current and noise performances [4].

The use of the PPD technology is envisaged in numerous space applications as well as in many other applications where ionizing radiation degrades the performances of image sensors. However, despite these superior performances compared to 3T photodiodes, PPDs are still sensitive to radiation induced degradation. Especially, total ionizing dose (TID) induced dark current increase and charge transfer efficiency degradations are a major limitation for the use of PPD CIS in harsh radiation environment [6], [7]. On the other hand, whereas many studies have proposed and validated radiation hardening techniques to improve the hardness of the conventional photodiode, no effective solution really exist today. Some tentative of PPD hardening design are proposed in literature such as the enclosed layout Transfer Gate (TG) design [8], [9], or the modulation of the shallow trench isolation recess distance. However, it appears that it does not improve efficiently the radiation hardness of the PPD [7], [9].

O. Marcelot, V. Goiffon and P. Magnan are with ISAE, Université de Toulouse, Image Sensor Research Team, 10 avenue E.Belin, F-31055, Toulouse, France. (corresponding e-mail: olivier.marcelot@isae.fr)

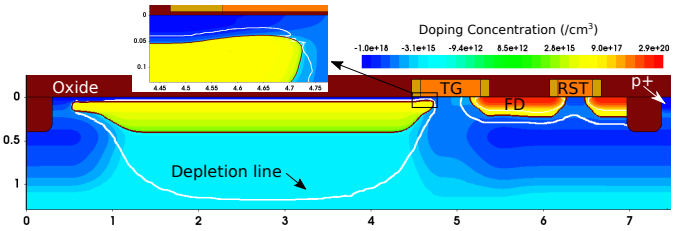

Fig. 1. TCAD doping distribution of the PPD. The white line represents the depletion limit after the PPD reset, TG being in accumulation ($V_{lowTG} = -0.8\ V$). An enlargement of the PPD extension under the TG spacer is shown for a better visualization of the depletion limit. Dimensions are given in μm.

The purpose of this work is to explore original PPD hardening technique options that can be easily integrated in a CIS process, by means of Technology Computer Aided Design (TCAD) simulations. In a first step, the TCAD simulator is calibrated according based on existing literature and experimental results. In a second step, a TCAD parameters giving an equivalent radiation fluence of 1 kGy, and 3 kGy are selected. Then, in the final part of this paper, various design and process hardening options are analyzed with respect to the PPD dark current behavior.

II. TCAD calibration

For all the work performed in this study, the Synopsys Sentaurus TCAD software is used. The 4T PPD is simulated in two dimensions, based on a submicrometer imaging process by means of Secondary Ion Mass Spectroscopy (SIMS) profiles implemented in the SDE tool. In addition to the TG, a reset transistor (RST) is added to the structure in order to ensure the N+ node floating (also called Floating Diffusion, FD), and a P+ contact is implemented inside the pixel (Fig. 1). With the aim to ensure the best charge transfer, it is assumed that the high pinning doping concentration is reduced under the spacer (see the discussion in [7]), likely due to the implantation step done after the spacer formation, leading to the rapprochement between the PPD extension and the surface oxide under the spacer. Therefore, a special attention is taken to reproduce this behavior in TCAD simulation by adjusting the TG spacer width, avoiding any contact between the surface oxide and the PPD extension (see the magnification in Fig. 1).

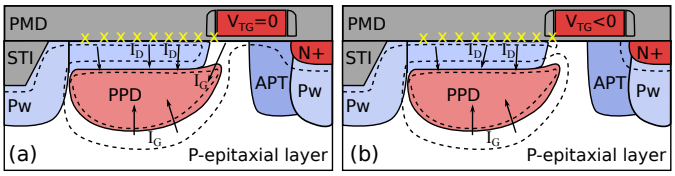

Fig. 2. Schematic view of 4T PPD pixels showing the different layers and the two main dark current sources, the diffusion dark current (I_D) and the generation dark current (I_G). (a) $V_{TG} = 0\ V$ and TG is depleted or it is negatively biased (b), the gate being accumulated. Yellow crosses represent the interface states or trapped charge activated in the dark current generation, and the dashed line is for the limit of depleted region.

The electrical simulations are conducted using Sdevice, with the Shockley Read Hall (SRH) recombination with the doping dependance, the Auger and Band to band tunneling models enabled. Moreover, the surface SRH recombination model is also enabled for all the silicon-oxide interfaces. At the beginning of the simulation, all contacts are set to 0 V and the PPD is at thermal equilibrium, allowing the eventual estimation of the equilibrium full well capacity (EFWC) [10]. Then, the reset drain is ramped up to 3.3 V and the PPD is depleted via the TG and RST gates. Once the PPD is depleted, the pinning voltage $\mathrm{V_{pin}}$ defined as the maximum deviation of the electron quasi-Fermi potential [11] may be extracted. Following this reset step, the PPD integrates in dark condition during 100 ms, and the dark electrons stored in the PPD are monitored.

A. Dark current sources

In photodiodes two main dark current sources may be identified [12], [13], the diffusion (I_D) and the generation (I_G) dark current (Fig. 2).

The diffusion dark current is coming from interface states at the silicon-dioxide interface. Although the PPD depleted region can be completely isolated from this interface if the TG is properly accumulated, they are still too close to be in thermal equilibrium despite the high P doping concentration [14], [15]. Because of that, some electron-hole pairs are generated by interface states (i.e. the net surface recombination velocity is not null), and emitted electrons may diffused though the pinning implantation and may be captured by the PPD. During ionizing radiation exposure, TID induces more interface states and the diffusion dark current increases. The other source of dark current, the generation dark current, occurs when the PPD interface states are located directly inside the depleted region, which is the case in TG depletion regime (Fig. 2 (a)). In accumulation regime, the PPD depletion region does not reach any interface before irradiation as mentioned previously. After exposure to TID, the presence of positive trapped charge in the oxide can create depleted region around the interface [16]. TID induces trapped charge in thick oxides, i. e. in the premetal dielectric (PMD) oxide on top of the PPD and in the TG spacer region, but induces very few trapped charge in the MOSFET thin gate oxide. Consequently, the PPD depleted region may be in contact with the PMD and the spacer interfaces after irradiation even when the TG channel is accumulated. Moreover, due to the electric field in the vicinity of the TG, it seems reasonable to assume that most of the radiation induced trapped charge is located near the TG spacer. This assumption combined with a generally lower pinning doping concentration under the spacer, leads to an enlargement of the depletion extension under the spacer [7] (Fig. 2 (b)). Once the depleted regions touch each other, the generation dark current rapidly increases with the defect concentration.

B. Simulation of the diffusion dark current

The electron current density at the top boundary of the PPD depletion region can be modeled by [14], [15]:

$$J_n = \frac{qn_i^2}{N_A} \times \frac{\frac{D_n}{L_n} sinh\left(\frac{x_{SiO2}}{L_n}\right) + S\, cosh\left(\frac{x_{SiO2}}{L_n}\right)}{cosh\left(\frac{x_{SiO2}}{L_n}\right) + S\,\frac{D_n}{L_n} sinh\left(\frac{x_{SiO2}}{L_n}\right)} \quad (1)$$

where q is the elementary charge, n_i is the intrinsic carrier concentration, N_A is the acceptor concentration, D_n is the electron diffusion coefficient, L_n is the electron diffusion length, S is the surface recombination velocity and x_{SiO2} is the distance between the top of the depletion region and the $\mathrm{Si/SiO_2}$ interface. The diffusion dark current induced by radiation attributed to an increase of interface states can be modeled by the increase of $S = \sigma_n \upsilon_{th} N_{it}$ [17], where σ_n is the mean capture cross section, υ_{th} the thermal velocity and N_{it} the interface state density. In this work, S in Sdevice is modified by the parameter S_0 as expressed in the following,

$$S = S_0 \left[1 + S_{ref} \left(\frac{N_i}{N_{ref}}\right)^{\gamma}\right] \quad (2)$$

where $N_{ref}$is the reference doping concentration, N_i is the doping concentration and γ a factor which is unmodified and equal to 1.

Based on experimental measurements performed on the technology used in this paper, the PPD dark current in accumulation regime is in the range of few $e^-.s^{-1}.\mu m^{-2}$ [7], [15] (see the Fig. 3). Surprisingly, without modification of the default Sentaurus parameter, the simulated dark current is higher than 7000 $e^-.s^{-1}.\mu m^{-2}$. In addition, this very high value occults the dark current increase due to the surface recombination variation. In order to reduce the dark current to a reasonable value, the electron minority lifetime is increased as done in [18]. Indeed, the diffusion dark current decreases with the increase of the minority carrier lifetime as shown in [19], [20]. In Sdevice, the minority carrier lifetime relation is defined as [21]:

$$\tau_n\left(N_A\right) = \frac{\tau_{max}}{1 + \left(\frac{N_A}{N_{ref}}\right)} \quad (3)$$

where $N_{ref} = 10^{16}\ cm^{-3}$ is a reference doping concentration, and $\tau_{max} = 10\ \mu s$. Consequently, the parameter τ_{max} is changed from 10 μs to 10 ms which gives a simulated dark current equal to 13 $e^-.s^{-1}.\mu m^{-2}$, in a more acceptable range compared to experimental data. This modification gives much higher lifetime values. Although it may be surprising, it is possible to find similar results in the literature, among the great dispersion of measurements and relationships [22], [23].

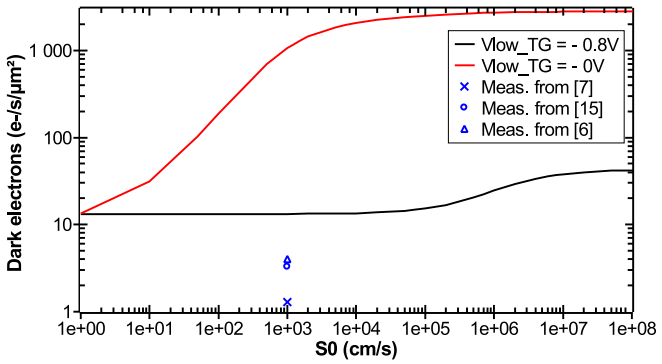

Fig. 3. TCAD simulation of the diffusion dark current for various surface recombination velocities and for $V_{TG} = -0.8\ V$ (black line) and for $V_{TG} = 0\ V$ (red line). Measurements in accumulation from [6], [7], [15] are added at $S_0 = 10^3\ cm.s^{-1}$ for comparison.

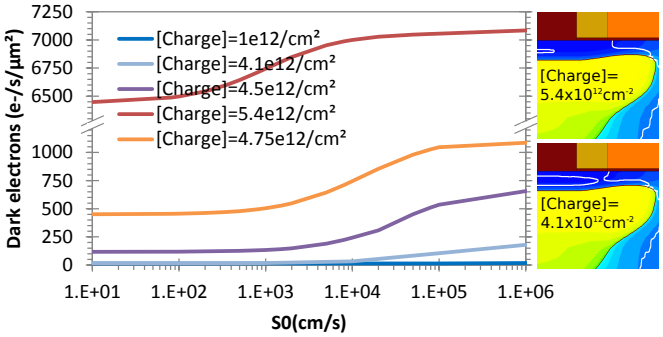

Fig. 4. TCAD simulation of the dark current for various surface recombination velocities S_0 at $V_{TG} = -0.8\ V$, and for several positive fixed charge densities at thick oxide - silicon interface. Next to the graph two doping distribution centered under the TG spacer are showing the white depletion limits for two positive fixed charge densities.

Fig. 3 displays the simulated dark current for various surface recombination velocities, the transfer gate being in accumulation regime for $V_{TG} = -0.8\ V$. At low surface recombination velocity the diffusion dark current is 13 $e^-.s^{-1}.\mu m^{-2}$, which is its minimum value. Then, from $S_0 = 10^5\ cm.s^{-1}$ the dark current increases until a saturation at 42 $e^-.s^{-1}.\mu m^{-2}$ achieved for $S_0 \geq 10^7\ cm.s^{-1}$. The same saturation of the dark current may be observed by means of the equation (1) [14]. For $V_{TG} = 0\ V$, the dark current is much higher, because of the contact between the PPD depleted region and the surface oxide which leads to an intense generation dark current.

C. Simulation of the generation dark current

SRH generation in depletion region under non-equilibrium condition is also an important dark current contribution in irradiated photodiodes. This radiation induced leakage current source is simulated by introducing a positive fixed charge sheet at the thick oxide - silicon interface, which excludes the gate oxide interface. Indeed, thanks to its reduced thickness, this latter oxide is not supposed to trap any significant fixed charge in the studied TID range. In addition, the fixed charge density is increased by 20 % in the TG spacer region, as explained in the introduction. The 20 % does not rely on measurement but it is used to facilitate the depletion under the spacer as supposed in [7].

TCAD results are displayed in the Fig. 4. Increasing the positive fixed charge concentration higher than $4 \times 10^{12}\ cm^{-2}$ strongly increases the dark current and especially when the surface recombination velocity is high. Indeed, below a charge concentration of $4.1 \times 10^{12}\ cm^{-2}$ the photodiode and interface depleted regions are well separated, leading to a dominant diffusion dark current contribution. Then, above a charge concentration of $4.1 \times 10^{12}\ cm^{-2}$, the PPD depletion extension touches the oxide depletion extension, the generation dark current appears and increases rapidly with the positive charge concentration. For a charge concentration higher than $5.6 \times 10^{12}\ cm^{-2}$ the PPD depletion extension reaches all the top thick oxide interface.

D. TCAD parameters selection

Our goal is to simulate a radiation fluence of 1 kGy, because it corresponds to the highest requirement for most space applications, and because this is the radiation dose level at which clear degradation of PPD parameters are reported in the literature. To achieve it, a comparison of measured dark current at $V_{lowTG} = 0\ V$ and $V_{lowTG} = -0.5\ V$ before and after a 1 kGy irradiation is done, by means of the data published in [6] for the same technology used in this work. Before irradiation, changing the condition $V_{lowTG} = -0.5\ V$ to $V_{lowTG} = 0\ V$ multiplies the measured dark current by 7, which is equivalent to the TCAD simulation with $S_0 = 50\ m.s^{-1}$. Following a 1 kGy irradiation, at $V_{lowTG} = 0\ V$ the dark current is increased by about 12 and at $V_{lowTG} = -0.5\ V$ it is increased by 40. Consequently, the parameter $S_0 = 10^3\ m.s^{-1}$ and the positive fixed charge concentration of $4.75 \times 10^{12}\ cm^{-2}$ should simulate the induced radiation effect at 1 kGy.

With the aim to go a little further, parameters simulating radiation effects at 3 kGy are used as a worst case condition. They are determined by $S_0 = 10^3\ m.s^{-1}$ and a positive fixed charge concentration of $5.4 \times 10^{12}\ cm^{-2}$.

III. Study of Hardening Options

In the following, several design and process hardening options are studied for the PPD by using the calibrated TCAD model presented in the previous section. V_{pin} and EFWC are extracted as described in the beginning of the previous section. The PPD transfer inefficiency (also called lag) is estimated by calculating the ratio of residual electrons in the PPD over the initial quantity after the charge transfer. The dark current before irradiation is simulated with $S_0 = 50\ cm.s^{-1}$ and no positive fixed charge. After irradiation, it is simulated with $S_0 = 10^3\ cm.s^{-1}$ and $S_0 = 10^4\ cm.s^{-1}$, and with positive fixed charge up to $5.4 \times 10^{12}\ cm^{-2}$.

Before irradiation, as shown by the Fig. 5, V_{pin} is 1 V, the EFWC is 3000 $e^-.\mu m^{-2}$, and the lag is simulated at 2×10^{-4}. In the following, if not stated otherwise, the lag keeps the same value. After a 1 kGy irradiation, the unmodified design (Ref in the Fig. 6) is showing a dark current multiplication of almost

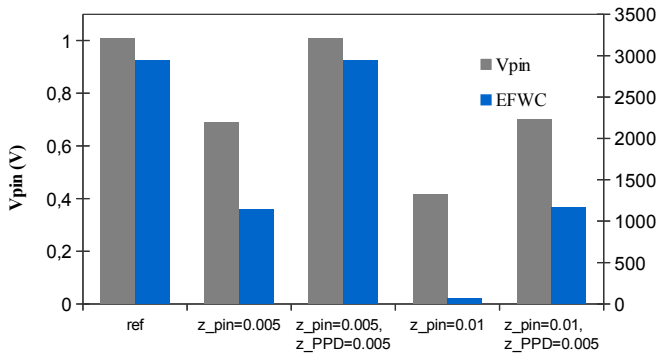

Fig. 5. TCAD simulation of the pinning voltage and the equilibrium full well capacity for various designs before irradiation. Ref is for reference, z_pin is the depth shift of the p pinning layer, z_PPD is the depth shift of the photodiode layer, both in μm.

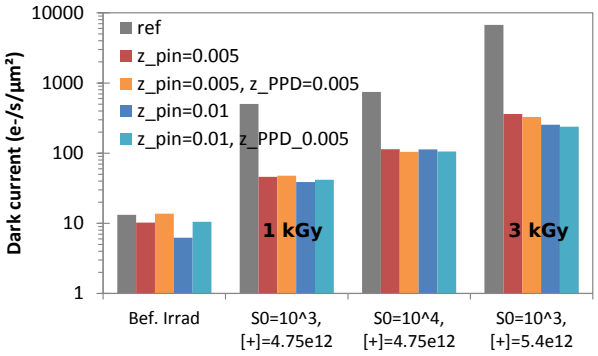

Fig. 6. TCAD simulation of the dark current before and after irradiation for various designs. Ref is for reference, z_pin is the depth shift of the p pinning layer, z_PPD is the depth shift of the photodiode layer, both in μm. S_0 is the surface recombination velocity in $m.s^{-1}$and $[+]$ is the positive fixed charge concentration in cm^{-2}.

40, as reported experimentally (section II-D), which provides an additional validation of the performed TCAD calibration.

A. Modification of photodiode implantation depths

The first attempt of hardened design consists in burying deeper the PPD, by extending the distance between the PPD and the surface oxide with the aim to prevent the spacer interface depletion region to reach the PPD depletion region. To do so, the depth of the p+ pinning layer and eventually the photodiode analytical profiles are respectively varied by the distance z_pin and z_PPD in μm. Although a unique p+ pinning depth shift may be sufficient, a photodiode depth shift is also studied in order to limit the effective PPD doping reduction due to the deeper pinning implantation. TCAD simulation results are displayed in Fig. 6 and in Fig. 5.

If only the p+ pinning depth is modified, the dark current at 1 kGy is divided by about 10, and at 3 kGy it is divided by 18 for z_pin $= 0.005$ μm and by 26 for z_pin $= 0.01$ μm. The thicker pinning layer leads to a deeper PPD depletion region, which delays its merging with the interface depleted region (see Fig. 7). The generation dark current is therefore reduced. While the dark current may be decreased by a deeper pinning layer, V_{pin} and the EFWC are seriously reduced. Thereby, the

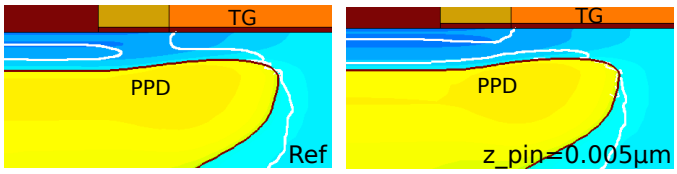

Fig. 7. TCAD simulation of the doping distribution after irradiation (equivalent 1 kGy). Ref is for the reference design, z_pin is the depth shift of the p pinning layer. The white line is the depletion limit.

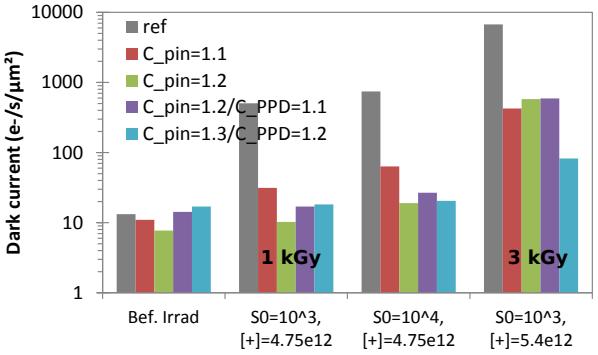

Fig. 8. TCAD simulation of the dark current before and after irradiation for various designs. Ref is for reference, C_pin is the concentration enhancement of the p pinning layer, C_PPD is the concentration enhancement of the photodiode layer. S_0 is the surface recombination velocity in $m.s^{-1}$and $[+]$ is the positive fixed charge concentration in cm^{-2}.

EFWC is divided by 3 with z_pin $= 0.005$ μm. Therefore, the depth of the photodiode layer is also increased to maintain original V_{pin} and EFWC values. The best result is obtained with z_pin $= 0.005$ μm and z_PPD $= 0.005$ μm, as the pinning voltage and the EFWC remains unchanged while the dark current is divided by 10 at 1 kGy.

Whereas the 1 kGy irradiation results in a dark current increase of 40 in TG accumulation regime, it is possible to find a combination of pinning and photodiode layer depths which leads to a dark current increase lower than 4. These modifications remain possible if the PPD implantation energies are slightly increased, which requests a process flow change but does not require the use of an extra mask.

B. Modification of photodiode implantation concentrations

This hardening technique relies on the same motivation, avoiding the merging of the depleted regions under the spacer, but with an enhancement of the doping concentration of the pinning layer and eventually of the photodiode layer. The effect is expected to be doubled: an enlargement of the pinning layer, and a reduction of the electron current density at the top boundary of the PPD depletion region due to the higher doping concentration of the pinning layer. The analytical doping profiles of the pinning and the photodiode layers are respectively enhanced by a factor C_pin and C_PPD. Similarly as before, the PPD doping concentration is eventually increased in order to compensate its effective reduction due to the pinning doping concentration enhancement.

Fig. 8 shows a dark current at 1 kGy divided by 16 at C_pin $= 1.1$ and slightly lower than the non-irradiated one

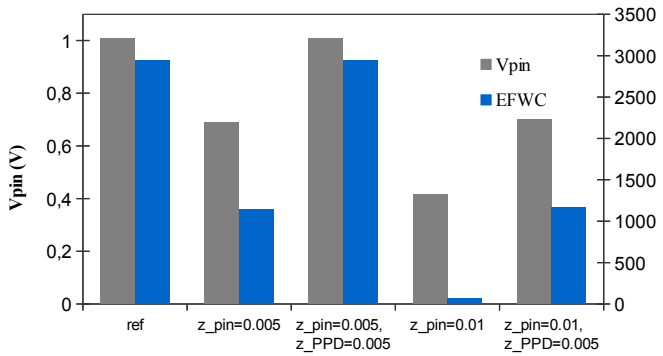

Fig. 9. TCAD simulation of the pinning voltage and the equilibrium full well capacity for various designs before irradiation. Ref is for reference, C_pin and z_PPD are respectively the concentration enhancement of the p pinning profile and of the photodiode profile.

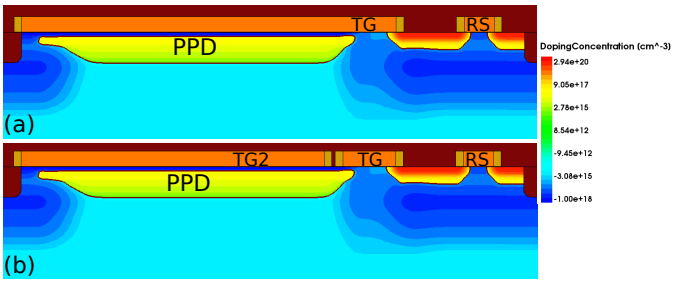

Fig. 10. TCAD two dimensional distributions of the doping concentration showing the simulated device with an enlargement of the TG gate over the PPD (a), and with an additional large gate over the PPD (b).

at C_pin $= 1.2$, which is a nice reduction compared to the previous attempt. The higher surface recombination velocity increases the dark current by 2 while it was increased by more than order of magnitude for the depth shifted pinning layer discussed in the previous section. This confirms the effect of a higher p+ doping concentration on the electron current density reduction at the PPD depletion boundary, as much less electrons are available at equilibrium. At 3 kGy, the dark current is divided by maximum 8. As expected, the main PPD characteristics are affected, and at C_pin $= 1.2$ V_pin is divided by 2 and the EFWC is divided by 8 (Fig. 9). If the PPD doping concentration is also enhanced, the dark current is not just greatly reduced but the pinning voltage and the EFWC are conserved. The best result is obtained with the following parameters, C_pin $= 1.3$ and C_PPD $= 1.2$, which allow a dark current divided by 80 at 3 kGy.

Increasing the pinning and the photodiode layer concentration allows a much smaller dark current multiplication after irradiation. In the best case, the dark current is only increased by less than 10% at 1 kGy (compared to 40 on the Ref PPD) and multiplied by 5 at 3 kGy. As for the previous case, it requires a process flow modification but no mask modification.

C. Poly-silicon over the PPD

The last radiation hardening solution explored consists in extending the poly-silicon TG gate over the PPD (Fig. 10 (a)). This solution corresponds to what is proposed in [7] except

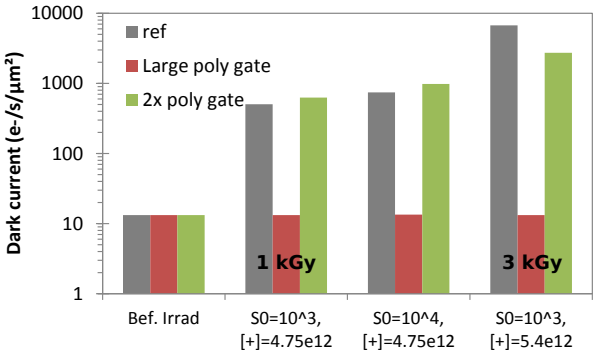

Fig. 11. TCAD simulation of the dark current before and after irradiation for various designs. Ref is for reference, *Large poly gate* is the design with TG gate over the PPD, *2x poly gate* is the design with an additional gate over the PPD, separated from TG. S_0 is the surface recombination velocity in $m.s^{-1}$and $[+]$ is the positive fixed charge concentration in cm^{-2}.

that here a single gate is used all over the PPD whereas two gates are mentioned in [7]. Using a single gate on top of the PPD instead of two solves the issue related to the presence of a dielectric in the gap between the two gates that could still trap some fixed charge. The integration of a poly-silicon gate over a photodiode in order to reduce radiation effects has already been tested in [24]. However, in [24], the partially PPD is contacted by means of a surface N+ implantation, and the PD depleted region touches the surface.

Due to the specific design, this sensor will exhibit higher performance if backside illuminated because of the presence of poly-silicon over the photo-sensitive area that will strongly reduces the quantum efficiency in the blue part of the spectrum if front-side illuminated. The goal is to keep a thin oxide all over the PPD as it is much less prone to trapping charge and interface state buildup. Indeed, a MOS transistor thin gate oxide in the studied technology node does not seem sensitive to radiation induced defects until 10 kGy [25]. Therefore, the simulation is performed without positive fixed charge at all silicon - oxide interface over the PPD. However, as a worst-case scenario, simulations are performed with modified surface recombination velocities at all silicon - oxide interfaces, as if interface states have been created.

The second benefit of this proposed solution if the fact that applying a negative voltage on the extended TG will allow to keep the Si/SiO2 interface accumulated even if some radiation induced defects are created in the gate oxide.

Fig. 11 shows the TCAD results for the dark current before and after irradiation. An enlarged TG gate over the PPD suppresses the dark current increase after irradiation, even at high fluence. Indeed, as no spacer and no thick oxide are in the vicinity of the PPD, there is no noticeable interface states and fixed charge leading to depletion extension. In addition, as no modification is done on PPD implantations, V_pin and the EFWC remain identical. However, the charge transfer is slightly degraded as the lag increases from 2×10^{-4} to 1×10^{-3} because of the TG bias during transfer which creates a vertical electric field in addition to the lateral electric field. If the large TG gate is separated in two gates (Fig. 10 (b)) as proposed in [7], the larger one over the PPD remaining at 0 V, the

transfer is not degraded but the dark current is as worse as the reference design because of the presence of thick oxide between the two gates. However, the two gates solution could be improved by reducing the gap between the two gates or by using process that allows the second gate to overlap the TG one in order to better control the potential in the gap and fight against the trapped positive charge in this region.

Among all the hardening options studied, the enlargement of the TG gate over the PPD remains the most promising one, as the dark current is not increased until 3 kGy. Moreover, this solution presents a significant benefit compared to the other two, it only requires to change the order of the PPD implants and the TG polysilicon deposition in the process flow to allow the creation of a PPD below the TG without adding a mask or modifying the process recipe.

IV. Conclusion

In this work, a TCAD simulation is calibrated in order to reproduce radiation induced dark current in a Pinned Photodiode pixel. To do so, the diffusion dark current increase is modeled by a surface recombination velocity enhancement. Then, the generation dark current is modeled by the introduction of positive fixed charge at all thick silicon-dioxide interfaces. These two models are calibrated according to experimental comparisons of dark current before and after irradiation, under TG depletion or accumulation regime.

Although a 1 kGy irradiation induces a dark current multiplication by 40 in accumulation regime on the reference design, it appears that a depth shift of the pinning layer leads to a dark current multiplication by less than 4. On the other hand, an enhancement of the pinning layer concentration limits the dark current increase by less than 10%. These modifications result in an effective photodiode N-doping reduction which has to be compensated by a depth shift or by a doping enhancement of the photodiode layer to keep the same full well as the reference design.

Then, the last option consisting in an extension of the transfer gate over the PPD leads to no dark current increase until 3 kGy and no pinning voltage and EFWC reduction, unlike the two first options discussed above. Hence, this option appears to be the one that brings the highest radiation hardness. However, as the poly-silicon covers the PPD, this option has to be restricted to backside illuminated sensors.

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